CLAIMS

1. A charge pump circuit comprising first and second transistors of a first type (P30, P31) controlled by first complementary signals, third and fourth transistors of a second type (N30, N31) controlled by second complementary signals, a first current source (I30) being placed between a higher voltage terminal (vdd) and a first electrode of the first and second transistors, a second current source (I31) being placed between a lower voltage terminal (gnd) and a first electrode of third and fourth transistors, the second electrodes of the first and third transistors being connected to the circuit output (O), the second electrodes of second and fourth transistors being connected to a reference node (I), the circuit output being connected to the input (E_1) of an interface circuit (1), the output of the interface circuit (S_1) being connected to the reference node, the interface circuit comprising two input branches (be1, be2) and one output branch (bs1), each branch being connected between upper (vdd) and lower (gnd) supply terminals, each input branch comprising a transistor (P1, N1) having its control electrode connected to the input of the interface circuit (E_1), one of the two other electrodes of the transistor being connected to one of the supply terminals, a current source (I1, I2) being placed between the other one of the supply terminals and an intermediate node (A_1, B_1) connected to the last transistor electrode, the output branch comprising two complementary transistors (N2, P2), having their control electrodes connected to the intermediary nodes of the two input branches, one of the electrodes of each of the complementary transistors being connected to the interface circuit output, the last electrode of each of the transistors being connected to a supply terminal.

2. An interface circuit comprising one or two input branches (be10; be20, be21) and one output branch (bs10; bs20), each branch being connected between upper (vdd) and lower (gnd) supply terminals, each input branch comprising a transistor (P11; N20, N21) having its control electrode connected to the input of the interface circuit (E_{10}; E_{20}), one of the two other electrodes of the transistor being connected to one of the supply terminals, a current source (I10; I20, I21) being placed between the other one of the supply terminals and an intermediary node (A_{10}; A_{20}, B_{20}) connected to the last

transistor electrode, at least one of the two input branches comprising one or several diodes connected between the intermediary node and the last transistor electrode of a considered branch, the output branch comprising two complementary transistors (N10, P12; N24, P20) having their control electrodes connected to the intermediary nodes of one of the input branches or to the circuit input, one of the electrodes of each of the complementary transitors being connected to the circuit output (S_{10}; S_{20}), the last electrode of each of the transistors being connected to a supply terminal.

3. The circuit of claim 1 or 2, wherein the transistors are CMOS transistors, the control electrode of a transistor being its gate, the two other electrodes being its source and drain, and wherein the output branch (bs1, bs10, bs20) comprises a PMOS transistor (P2, P12, P20) and an NMOS transistor (N2, N10, N24), the drains of the PMOS and NMOS transistors being connected to the interface circuit output (S_1, S_{10}, S_{20}), the source of the PMOS transistor being connected to the upper supply terminal (vdd), the source of the NMOS transistor being connected to the lower supply terminal (gnd).

4. The circuit of claim 3, wherein the source of each of the circuit transistors is connected to the transistor substrate.

5. The circuit of claim 1 or 2, wherein the transistors are bipolar transistors, the control electrode of a transistor being its base, the two other electrodes beings its emitter and collector.

6. The interface circuit of claim 2 or 3, having a single input branch, the input branch (be10) comprising a PMOS transistor (P10) having its drain connected to the lower terminal (gnd) and its gate connected to the input of the interface circuit, the source of the PMOS transistor being connected to a cathode of a diode (P11), the current source of the input branch being placed between the anode of the diode and the upper supply terminal (vdd), the gate of the NMOS transistor (N2) of the output branch (bs1) being connected to the source of the PMOS transistor (P10) of the input branch (be10), the gate

of the PMOS transistor (P2) of the output branch (bs) being connected to the circuit input.

7. The interface circuit of claim 2 or 3, comprising first and second input branches, the first input branch (be20) comprising an NMOS transistor (N20) having its drain connected to the upper supply terminal (vdd), the current source (I20) of the first input branch being placed between the source of the NMOS transistor of the first input branch and the lower supply terminal (gnd), the second input branch (be21) comprising an NMOS transistor (N1) having its drain connected to the upper supply terminal (vdd), the source of the NMOS transistor (N21) of the second branch being connected to the anode of a first diode (N22), the cathode of the first diode being connected to the anode of a second diode (N23), the current source (I21) of the second input branch being placed between the cathode of the second diode and the lower supply terminal, the gates of the NMOS transistors of the first and second input branches being connected to the input (E_{20}) of the interface circuit, the gate of the NMOS transistor (N24) of the output branch (bs20) being connected to the source of the NMOS transistor of the first input branch, the gate of the PMOS transistor (P20) of the output branch being connected to the cathode of the second diode.

8. A charge pump circuit of claim 1 or 3, wherein the first and second transistors (P30, P31) are PMOS transistors and the third and fourth transistors (N30, N31) are NMOS transistors, and wherein the interface circuit comprises first and second input branches (be1, be2), a first input branch (be1) comprising a PMOS transistor (P1) having its drain connected to the lower supply terminal (gnd), the current source (I1) of the first input branch being placed between the source of the PMOS transistor of the first input branch and the upper supply terminal (vdd), the second input branch (be2) comprising an NMOS transistor (N1) having its drain connected to the upper supply terminal, the current source (I2) of the second input branch being placed between the source of the NMOS transistor and the lower supply terminal (gnd), the gates of the NMOS and PMOS transistors of the first and second input branches being connected to the interface circuit input (E_1), the gate of the NMOS transistor (N2) of the output branch

(bs1) being connected to the source of the PMOS transistor of the first input branch, the gate of the PMOS transistor (P2) of the output branch being connected to the source of the NMOS transistor of the second input branch.